Area Efficient Digital Logic Circuits Based On 5-Input Majority Gate Using QCA

# Summary

Many methods for fabrication of QCA basic cells are suggested such as metal island, magnetic, semiconductor, and molecular QCA. As is discussed in, metal dot implementations have proven to be the most successful material systems which are based on ‘single-electron transistors ‘fabrication techniques. Cowburn's group firstly proposes the magnetic implementation and extended by the Porod group and the Bokar group. In the physical semiconductor implementation, the Cavendish group of Smith et al. proved QCA operation in GaAs/AlGa As hetero structures with confining top-gate electrodes and the group of Kern et al. demonstrated a silicon QCA cell by employing an etching technique to form the dots.

Although many Researchers are concentrated to implement the logic gates and sequential elements. Most of the existing structures are constructed with 3-input majority gates and inverters. In the existing work the XOR gate and XNOR gates are implemented by using 3-input majority gate based 2:1 multiplexer. The QCA schematics and cell layouts of XOR and XNOR gate are displayed. The construction of XOR gate requires three 3-input majority gates and 40 cells and 3 clock zones. In the same way, XNOR gate also requires a similar number of majority gates, cells and clock zones for its building.

the XOR gate have 33.33% reduction in gate count, 30% decrease in the cell count with the same delay compared to existing design [XOR gate] because the existing design requires three majority gates and the proposed design requires only two majority gates for its construction. The similar improvements can be achieved in XNOR gate. Both logic gates have a delay of 3 clock zones similar to previous designs with reduced gates and cells. Similarly, in D-latch gate count is reduced by 33.33% and 25% improvements in clock zones and a lesser improvement in cell count can be achieved compared to existing design [D-latch]. The T-latch has 33.33% reduced gate count, 17% in cell count, and 25% in clock zones can be achieved compared to existing design [T-latch]. Likewise, the D flip-flop also has same gate count similar to D-latch, 16% reduction in cell count and 50% improvements in clock zones can be achieved compared to existing design [D flip-flop]. The simulation results of XOR gate is shown in Fig. 13. In QCA circuit, one complete clock cycle contains four clock zones titled as clock 0, clock 1, clock 2, and clock 3. As seen from the Fig. 13, it is evidently shown that the functionality of XOR gate and XNOR gate is correct, and the exact output appears in third clock zone (clock 2).